GOA UNIVERSITY
Taleigao Plateau, Goa 403 206

Course : RC 2016-17

RESULT REGISTER FOR B.E EXAMINATION HELD IN ELECTRONICS & TELECOMMUNICATION ENGINEERING FOR 5th SEMESTER MAY 2019 EXAM

COLLEGE : GOA COLLEGE OF ENGINEERING

SEAT No	P R No	GENDER	Attempts	NAME OF CANDIDATE / PAPER DESCRIPTION	THEORY		SESSIONAL	TERM WORK	TOTAL	PRACTICAL		ORAL	TOTAL		REMARKS
39	201610652	M	2	AIGAL ABHAY CHANDRAKANT											
				Digital Signal Processing	43		11	22	76 +						
				Transmission Lines and Antennas	40		14		54 +						
				Control System Engineering	42		14		56 +						
				Embedded Systems	59		11		70 +	10 +					
				VLSI Design and Technology	62		21		83 +	20 +					
				Analog Communication	0		12		12 A			17 P			
													398		F
40	201704559	F	2	AKALWADI ASHVINI SATYAPPA											
				Digital Signal Processing	40		10	22	72 P						
				Transmission Lines and Antennas	6		15		21 F						
				Control System Engineering	38	$2	15		53 P	$2					
				Embedded Systems	55		15		70 P		13 P				
				VLSI Design and Technology	52		15		67 +		16 +				
				Analog Communication	38	$2	10		48 +	$2		13 +			
													373	$4	F
42	201610553	F	2	DESAI TANVI SANJAY											
				Digital Signal Processing	49		10	22	81 +						
				Transmission Lines and Antennas	36	$4	12		48 P	$4					
				Control System Engineering	46		15		61 P						
				Embedded Systems	50		14		64 +		10 +				
				VLSI Design and Technology	64		10		74 +		16 +				
				Analog Communication	50		15		65 +			21 +			
													440	$4	P
43	201610554	M	2	DESSAI DIGVIJAY MARUTI											
				Digital Signal Processing	47		11	22	80 P						
				Transmission Lines and Antennas	35	$5	16		51 +	$5					
				Control System Engineering	40		13		53 +						
				Embedded Systems	51		6		57 +		11 +				
				VLSI Design and Technology	52		10		62 +		18 +				
				Analog Communication	51		10		61 +			21 +			
													414	$5	P
44	201704558	F	2	EKAWADE PRANALEE JAIPRAKASH											
				Digital Signal Processing	40		10	21	71 +						
				Transmission Lines and Antennas	40		12		52 P						
				Control System Engineering	0		18		18 A						
				Embedded Systems	42		10		52 P		13 P				
				VLSI Design and Technology	60		10		70 +		20 +				
				Analog Communication	53		10		63 +			13 +			
													372		F
45	201610566	F	2	GAONKAR DEEPTI DHARMA											
				Digital Signal Processing	55		13	20	88 +						
				Transmission Lines and Antennas	54		20		74 +						
				Control System Engineering	43		14		57 P						
				Embedded Systems	60		11		71 +		10 +				
				VLSI Design and Technology	73		15		88 +		20 +				
				Analog Communication	51		16		67 +			18 +			
													493		P
46	201610779	M	2	JOY PAHARI											
				Digital Signal Processing	68		14	20	102 +						
				Transmission Lines and Antennas	38	$2	16		54 +	$2					
				Control System Engineering	41		10		51 +						
				Embedded Systems	49		13		62 P		18 P				
				VLSI Design and Technology	53		18		71 +		22 +				
				Analog Communication	51		15		66 P			14 P			
													460	$2	P
47	201610577	M	2	KAVALEKAR ABHIJIT SHASHIKANT											
				Digital Signal Processing	45		12	21	78 +						
				Transmission Lines and Antennas	41		16		57 +						
				Control System Engineering	38	$2	12		50 P	$2					
				Embedded Systems	61		12		73 +		11 +				
				VLSI Design and Technology	72		16		88 +		20 +				
				Analog Communication	51		9		60 +			12 +			
													449	$2	P

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COLLEGE : GOA COLLEGE OF ENGINEERING

SEAT No	P R No	GENDER	Attempts	NAME OF CANDIDATE / PAPER DESCRIPTION	THEORY	SESSIONAL	TERM WORK	TOTAL	PRACTICAL	ORAL	TOTAL	REMARKS
48	201610776	M	2	MOHNISH P NAIR								
	Digital Signal Processing				57	10	22	89 +				
	Transmission Lines and Antennas				50	16		66 +				
	Control System Engineering				43	9		52 P				
	Embedded Systems				46	10		56 +	11 +			
	VLSI Design and Technology				70	14		84 +	20 +			
	Analog Communication				44	9		53 +		16 +		
											447	P
49	201705126	F	2	NAIK GANDHALI DATTARAM								
	Digital Signal Processing				47	7	21	75 +				
	Transmission Lines and Antennas				38	$2 10		48 +	$2			
	Control System Engineering				0	15		15 A				
	Embedded Systems				64	12		76 +	10 +			
	VLSI Design and Technology				76	10		86 +	16 +			
	Analog Communication				57	12		69 +		16 +		
											411	$2 F
51	201704561	F	2	POLEM REDDY SONALI VENKATA RAMANA								
	Digital Signal Processing				47	10	24	81 +				
	Transmission Lines and Antennas				38	$2 16		54 +	$2			
	Control System Engineering				35	$5 17		52 P	$5			
	Embedded Systems				55	16		71 +	12 +			
	VLSI Design and Technology				60	16		76 +	16 +			
	Analog Communication				41	18		59 +		15 +		
											436	$7 P
52	201610755	M	2	PRATIK SINGH NEGI								
	Digital Signal Processing				35	$5 11	21	67 +	$5			
	Transmission Lines and Antennas				50	13		63 P				
	Control System Engineering				35	$5 14		49 P	$5			
	Embedded Systems				41	13		54 P	14 P			
	VLSI Design and Technology				66	13		79 +	17 +			
	Analog Communication				52	12		64 +		15 +		
											422	$10 P
53	201610782	F	2	SAHANA RAMESH BELLAD								
	Digital Signal Processing				51	11	22	84 +				
	Transmission Lines and Antennas				50	14		64 +				
	Control System Engineering				49	16		65 +				
	Embedded Systems				62	13		75 +	10 +			
	VLSI Design and Technology				80	16		96 +	20 +			
	Analog Communication				69	11		80 P		14 P		
											508	P
54	201610621	M	2	SHAIKH ABDUL KADER								
	Digital Signal Processing				43	8	22	73 +				
	Transmission Lines and Antennas				35	$5 14		49 +	$5			
	Control System Engineering				35	$5 12		47 +	$5			
	Embedded Systems				40	14		54 +	10 +			
	VLSI Design and Technology				52	11		63 +	20 +			
	Analog Communication				54	15		69 P		12 P		
											397	$10 P
55	201711499	M	2	SONTI GIRISH IRANNA								
	Digital Signal Processing				44	7	22	73 +				
	Transmission Lines and Antennas				47	19		66 +				
	Control System Engineering				41	13		54 P				
	Embedded Systems				56	15		71 +	13 +			
	VLSI Design and Technology				61	11		72 +	20 +			
	Analog Communication				54	17		71 +		18 +		
											458	P

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SEAT No	P R No	GENDER	Attempts	NAME OF CANDIDATE
56	201610635	M	2	VELIP ADHITYA PANGLO

PAPER DESCRIPTION	THEORY	SESSIONAL	TERM WORK	TOTAL	PRACTICAL	ORAL	TOTAL	REMARKS
Digital Signal Processing	41	10	22	73 +				
Transmission Lines and Antennas	36 $4	11		47 +	$4			
Control System Engineering	35 $5	14		49 P	$5			
Embedded Systems	40	10		50 +	10 +			
VLSI Design and Technology	62	12		74 +	18 +			
Analog Communication	53	12		65 +		13 +		
							399 $9	P

Read By :

Checked By :

Date :

Assistant Registrar-E(Proff.) Controller Of Examinations Registrar

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